Variable Hardware Inductance Simulator

Submitted To

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EXECUTIVE SUMMARY

This report documents the design and implementation of a variable hardware inductance simulator during the spring 2006 semester. This project was completed at the Institute for Advanced Technology for the purpose of research in the field of pulsed-power applications. Included are the design schematics and implementation details used to create a ‘black box’ capable of simulating a user-defined inductance between 100mH and 10H to an accuracy of 5%. The deliverable simulates an inductor for inputs between -120V and 120V with up to 20A of current at frequencies below 1 kHz.

The implementation process involved two competing designs based around the same basic circuit. The first employed a switching MOSFET to control the current, while the more favorable design used a bipolar junction transistor operating in the linear region. The latter design was chosen to be implemented on the full power scale.

The testing process was completed using a desktop power supply controlled by an isolated waveform generator. The simulator performed within 5% of the ideal input current for a variety of pulse shapes and lengths longer than 1msec. In order for the first 10msec of the input current to match the integration of the forst 10msec of the input voltage, an all-time bias current of 10-20mA is necessary. Therefore, except for the initial DC current, the product met specifications within its operating bandwidth.

The project cost \$5028, and was \$190 under budget. The project met all time and monetary restrictions; although, it involved more professional expertise than was initially estimated.

All relevant safety and ethical considerations have been addressed, and the deliverable is ready for integration into its application area.

1.0 INTRODUCTION

This document will describe the process of implementing the variable hardware inductance simulator as well as the proposed schedule and cost estimate.

For the past two years, synchronous alternators have been implemented at the Institute for Advanced Technology (IAT) as pulsed-power sources. These machines are being considered as power supplies for electromagnetic launchers, rail guns. One of the attractive characteristics of the pulsed alternators is the ability to quickly exchange mechanical energy for electrical, and vice-versa.

In order to experiment with transferring electrical energy out of the machines and subsequently recovering that energy back into mechanical energy, a hardware electrical energy-storage unit is needed. Large-scale inductors (100mH – 10H) are expensive to build, inefficient, take up space, and researchers are unable to quickly change their inductance values. I used my electrical engineering education and my experience with power electronics to design and build a variable hardware inductance simulator during the spring 2006 semester.

The following report describes the simulator, describes the process of design and implementation, examines the quality of the deliverable, and reviews the costs and safety considerations.

2.0 DESIGN PROBLEM STATEMENT

In order to increase the efficiency of the rail gun's pulsed power supply, it is desirable to place a large inductance in parallel with the power supply that will charge during the firing sequence and then recharge the generator afterwards. The value of this inductance is between 100mH and 10H, depending on the physical aspects of each gun/generator pair, and the inductor must tolerate currents as high as 20 amps. Because the fabrication of aircore inductors of this size and power would be very expensive, large, and difficult to adjust, it is desireable to build a variable hardware inductance simulator.

The final deliverable is one variable hardware inductance simulator capable of simulating 100mH-10H, specified by a user-controlled potentiometer, which can handle an input of up to 120V and 20A of DC current, at a frequency between DC and 360Hz. This 'black box' has two input/output nodes, one for each end of the 'inductor,' and a potentiometer to adjust the value of the 'inductor.' The goal of this project is for the simulated inductor to act indistinguishably from an inductor within the absolute maximum ratings.

Because the current through an inductor is an expression of the integration of the voltage across its terminals with respect to time, the design approach centered around the implementation of a voltage integration circuit, and much of the design time was spent finding the most desirable transducer from that voltage into load current.

3.0 DESIGN PROBLEM SOLUTION

The implementation of the variable hardware inductance simulator is described by three important design modules. First, the input voltage integration circuit is designed to generate a control voltage which represents the input current function with respect to time. Second, a current sensing circuit provides error feedback to the control loop and scales the magnitude of the current according to the user's desired inductance value. Finally, the resulting error-corrected cvontrol voltage is transduced into an input current.

3.1 VOLTAGE INTEGRATION CIRCUIT

In order to generate an integration voltage, a simple RC network combined with an operational amplifier was implemented (See Figure 1). A 100:1 voltage divider was necessary in order to avoid saturating the operational amplifier, as an input voltage higher than 15V could damage the amplifier. The 20kΩ resistor and 1uF capacitor define the integration parameters. The 4.7MΩ resistor allows Vout to return 0V if Vin is constantly

0V with a long time constant of 4.7 seconds[1]. Ignoring this bleed resistor for any frequency above 0.2Hz, the output voltage is proportional to the integral of the input voltage according to the following equations[1]:

$$V_{out} = -(1/(100*(20k\Omega)*(1uF)))*\int V_{in}(t)dt$$
$$V_{out} = -0.5*\int V_{in}(t)dt$$

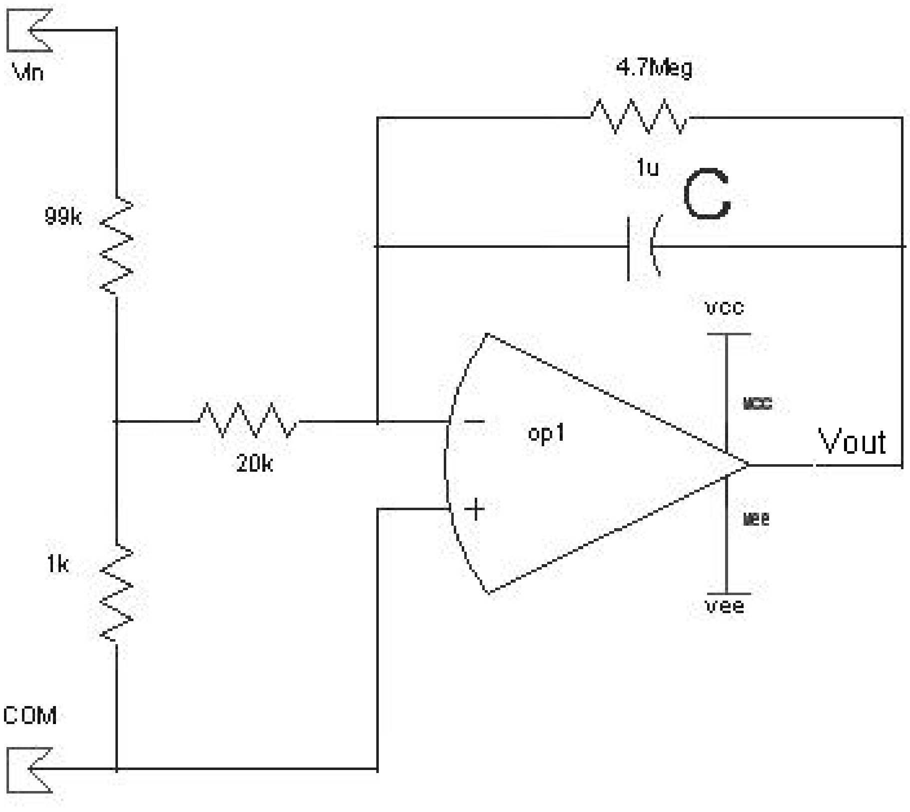

Figure 1. Voltage Integration Circuit

3.2 CURRENT SENSING CIRCUIT

The second design module of the variable hardwave inductance simulator is an error signal generated by the current sensing cicuit (See Figure 2). This circuit is an adjustable-gain amplifier of the voltage across a 0.01Ω current sensing resistor; it measures the current and scales the error signal according to the user's input Radj[2]. Vout varies according to the following equations[2]:

$$\text{Vout} = -(47\text{k}\Omega/\text{Radj})*(0.01\Omega*\text{Iin})$$
$$\text{Vout} = -(470\Omega/\text{Radj})*\text{Iin}$$

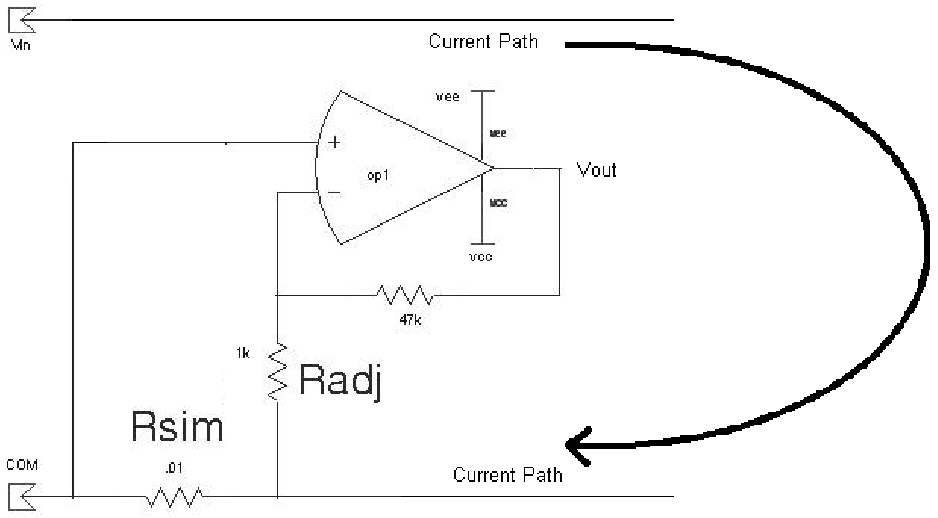

Figure 2. Current Sensing Circuit

3.3 CONTROL VOLTAGE TO CURRENT TRANSDUCER

After the control voltage is error-corrected, it must be transduced into an input current in four stages. First, the signal must be isolated and centered at the linear transistor's emitter voltage in order to appropriately control the base. Second, the signal must be low-pass filtered to account for closed-loop propagation delay. Third, the voltage must be linearly transduced into an input current by means of a bipolar junction transistor (BJT). Finally, the BJT must be biased so that it will not stop conducting when the input voltage is negative.

3.3.1 Isolation Amplifier

The control voltage is error-corrected on the non-isolated side of the ISOAD210 amplifier and sent through the isolation amplifier configured with unity gain (See red box in Figure 3). The ISOAD210 supports input.output isolation up to 2kV, and the output is attached through aa ground plane to the emitter of the BJT.

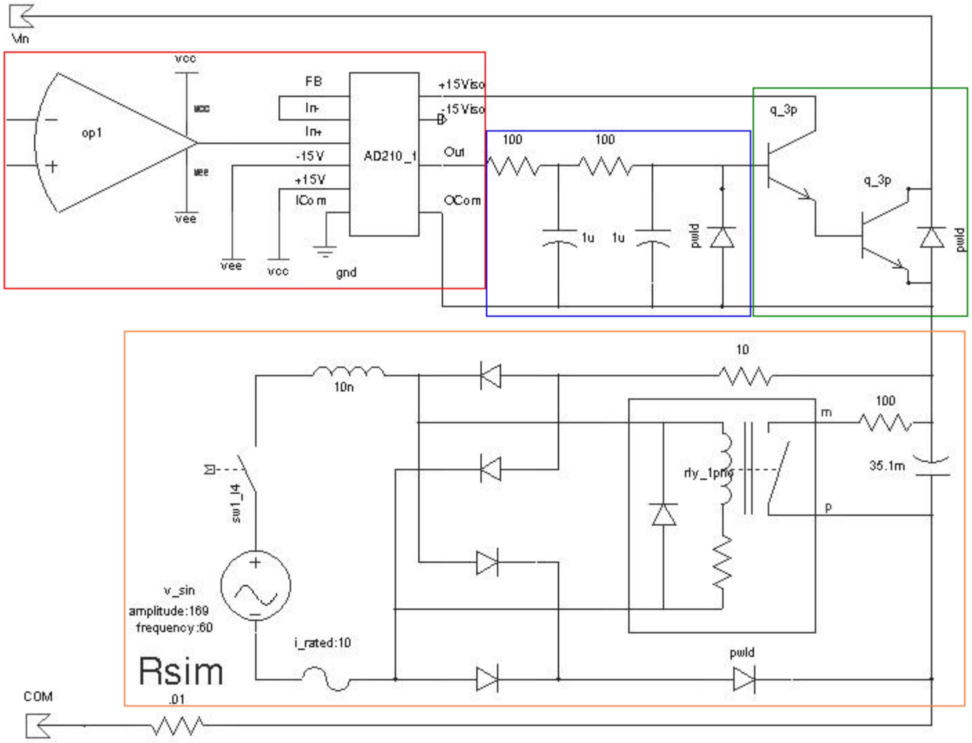

Figure 3. Control Voltage to Current Transducer

3.3.2 Low-pass Filter

Because the isolation amplifier has a propagation delay of about 20usec, the closed-loop propagation delay is significant. Without filtering, this delay causes the error-correcting section of the loop to overcompensate while it waits for the isolation amplifier to adjust its output. This produces an undesirable ringing at about 50kHz (See Figure 4). To compensate for this cosed-loop delay[2], a double-pole low-pass filter with a rolloff frequency of 1.6kHz is implemented at the output of the isolation amplifier (See blue box in Figure 3). Because any base voltage lower than the themal voltage of the BJT will cause current shutoff, an emitter-base diode is implemented to keep the control voltage from drifting too far below the thermal voltage (See blue box in Figure 3).

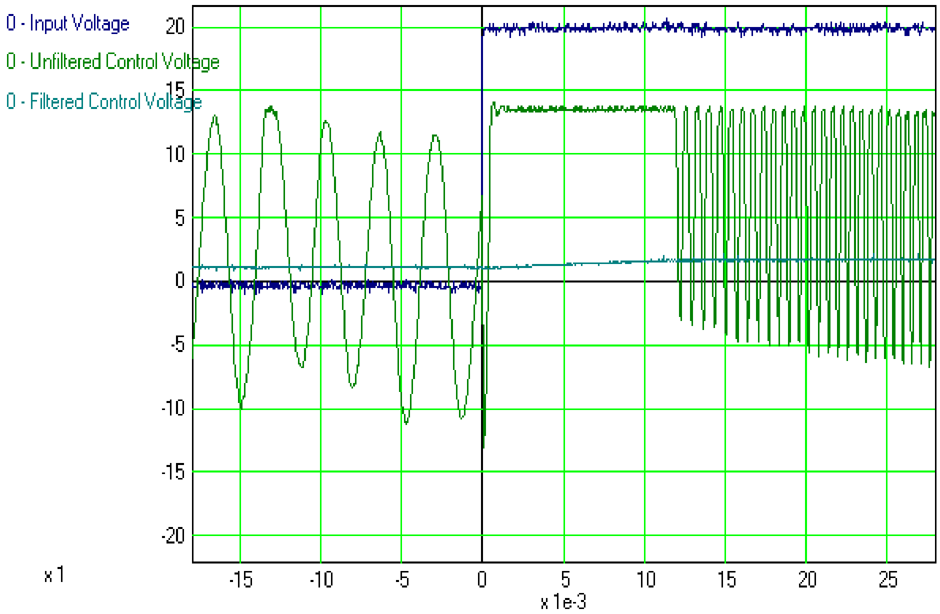

Figure 4. Results of Filtering the Control Voltage

3.3.3 Voltage to Current Transducer

Cascaded BJTs are implemented in order to attain the necessary current gain (See green box in Figure 3). Because the output transistor is rated for 400W, its current gain is only 120, so a second BJT is necessary to allow currents up to 20A[3]. An intrinsic diode protects the output transistor from accidental reverse-bias conditions.

An alternate design was simulated and implemented using pulse width modulation to control a MOSFET in the interest of reducing transistor heating and energy losses (See Figure 5). However, a series power resistor was required to drop the input voltage, and any resistance low enough to allow 20A was not high enough to overshadow the 3Ω input source resistance[4]. Also, high switching transients and ground noise disruption discouraged further experimentation.

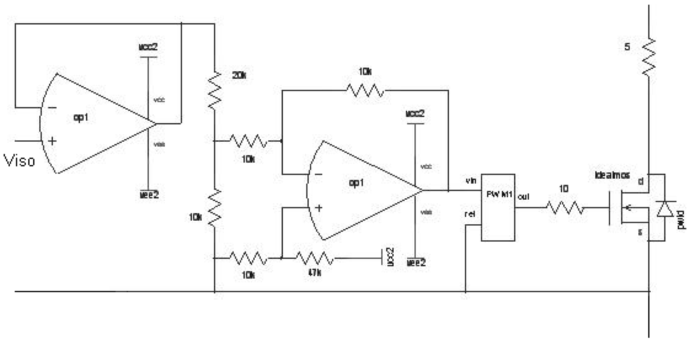

Figure 5. Alternate Switching Voltage to Current Transducer

3.3.4 Transistor Biasing Power Supply

When Vin is negative with respect to COM, it may atill be necessary to force a positive input current in order to accurately simulate an inductor. To keep the BJT forward-biased, a power supply that forces the emitter voltage lower than the lowest possible input voltage (-120V) is necessary (See orange box in Figure 3). This supply is powered from a standard 60Hz, 120Vrms wall outlet. An input resistor of 10Ω limits the current to about 10A when the network is fully charged, and a fast-acting 10A fuse insures that less than 10A is drawn from the wall outlet. Because of the large energy storage in a 35mF capacitor network at 170VDC, a safety relay is implemented that will drain the energy through a 100Ω resistor when the power is turned off.

4.0 DESIGN IMPLEMENTATION

The preliminary design of this circuit was done via a circuit simulation program called Saber, which allowed me to accurately model each circuit component and provided useful time-domain and frequency analysis at each step in the design process. Originally, it was designed to be a true bipolar inductance simulator, capapble of forcing forward or reverse current regardless of input voltage polarity. However, in order to implement this circuit, it was necessary to construct a second power supply to ensure proper transistor biasing. The cost of this supply was weighed against the marginal benefit of the bipolar operation, and my employer decided to adjust the original criteria to exclude reverse-current operation. The justification for this choice is that the application of this inductor would require a rectifier in series with the inductor, removing the need for reverse current simulation (See Figure 6).

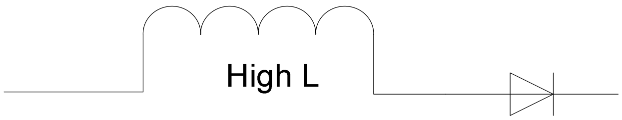

Figure 6. Representation of Unipolar Inductance Simulation

Another important modification to the original design was the addition of a DC offset control potentiometer to the intergrator op-amp. By modifying the DC offset, the baseline input current for an input voltage of zero can be calibrated. Ideally, this current value would be zero; however, I found that it was desirable to calibrate the circuit for 10-20mA of on current in order to keep the BJT conducting. If calibrated to zero current, the circuit can take as long as 10msec to forward bias the base-emitter (See Figure 7). In this way, the circuit does not meet the specification of simulating an ideal inductor; however, no other reasonable improvement could be found.

Similarly, the time constant of the integrator is 4.7 seconds instead of the infinite time constant of an idal inductor; however, resistivity in any known inductor of this size would create a time constant much lower than 4.7 seconds. Thus, the circuit does meet specifications with regard to time constant.

Originally, the criteria for frequency response of the inductance simulator were not clear, although the maximum frequency of the application is 360Hz. Because of the double-pole low-pass filter at 1.6kHz, the inductor cannot be relied on to perform accurately at input frequencies above 1kHz[3]. This does not necessarily contradict specifications; however, it is important to document this limitation.

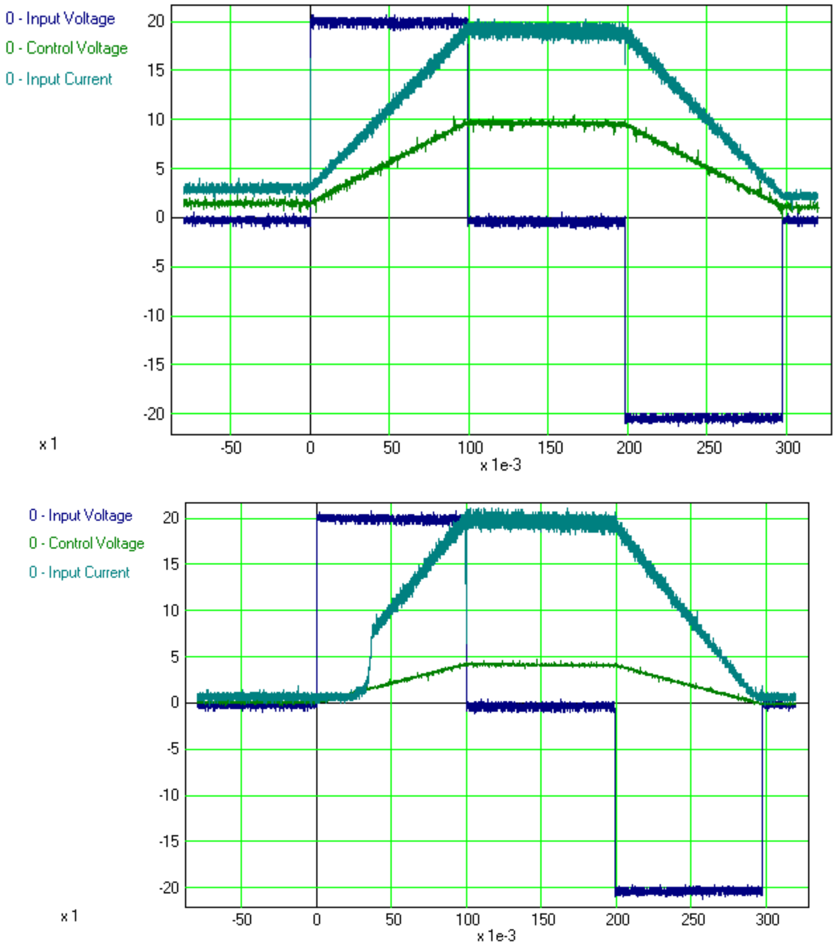

Figure 7. Calibrated Intergrator (Top), Uncalibrated Integrator (Bottom)

5.0 TEST AND EVALUATION

In order to test this circuit, I used an oscilloscope and a set of isolated, differential probes to avoid ground loop problems. A laptop connected to a National Instruments digital to analog converter (DAC) created a test signal which was passed as a control input to a high-power Kepco power supply. The Kepco supply has a gain of -5, so I was able to test inputs up to 50V and 8A. I used a differential probe to measure the input voltage trace, the control voltage trace, and the voltage across a current sensing resistor in series with the Kepco. By comparing the relationship between the input voltage and current, I was able to determine the effectiveness and accuracy of the variable hardware inductance simulator for a series of different pulse shapes and lengths (See Figures 7 - 10).

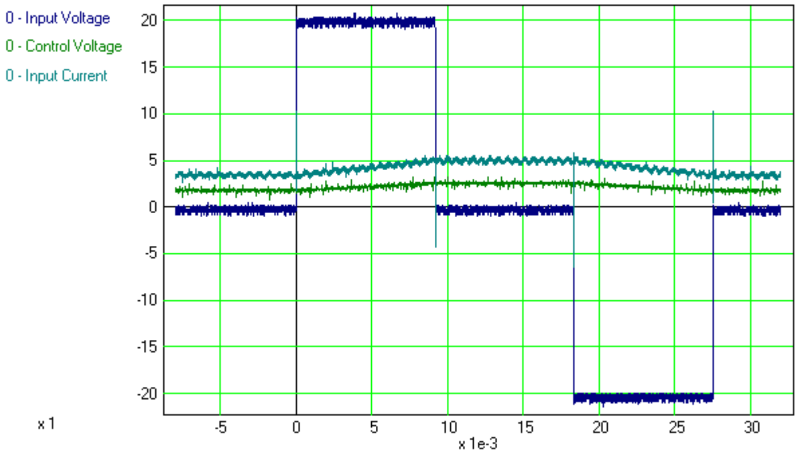

Figure 8. Example of 10ms Pulse Measurement

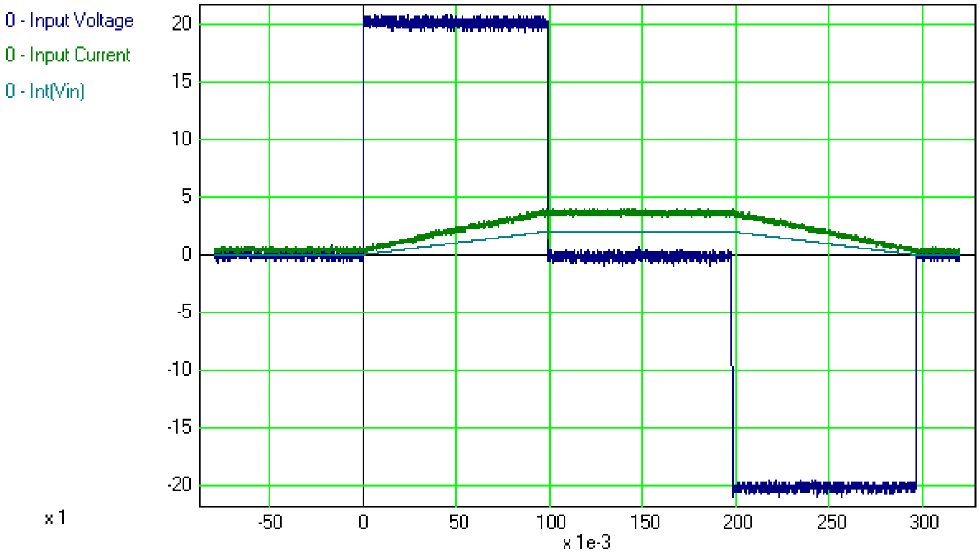

Figure 9. Example of 500mH Inductance Simulation

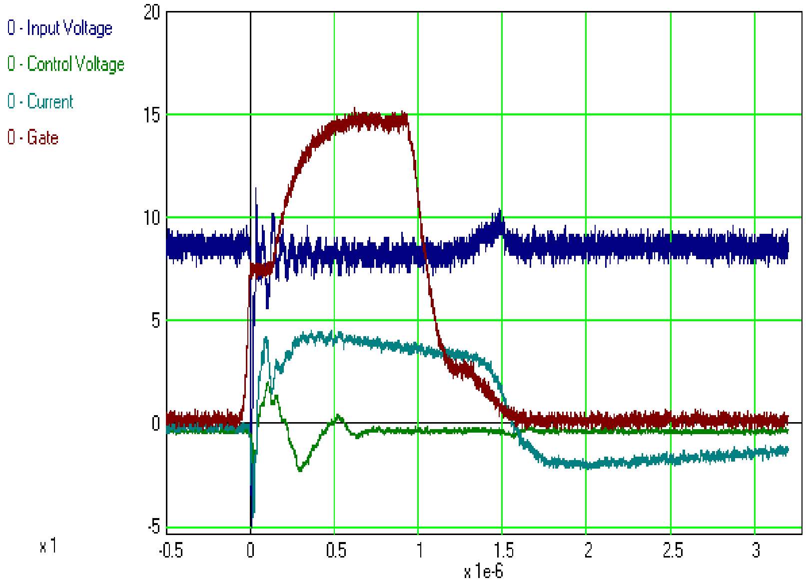

Figure 10. Measurement of Switching Circuit Parameters

Taking the difference between the recorded data from the hardware inductance simulator and a simulated ideal inductor, I observed less than 5% difference in input current in any pulse shape after the first millisecond. The hardware inductance simulator has larger differences in initial turn-on current during the first millisecond, but afterwards it accurately represents the integral of the input voltage. As the resistance of the adjustable potentiometer is remarkably consistant, the inductance simulator performs just as accurately over its entire range of inductance. One drawback of the design is that the simulated inductance varies inversely with the input potentiometer value, so it is very sensitive near the 10H end of the spectrum.

Besides testing the linear circuit, several tests with differential probes on the switching circuit showed ground plane problems and eventually indicated why the linear transistor design was preferable (See Figure 10).

6.0 TIME AND COST CONSIDERATIONS

Evaluating the cost of this project with respect to the initial estimate shows a favorable result. By overestimating initital costs and allowing for mistakes and replacement costs, my initial estimate was almost $200 higher than the actual cost. Because the anticipated costs were acceptable to attain a working hardware inductance simulator, the actual cost is similarly acceptable and very agreeable.

The project met all of its time and budget constraints. In actuality, this project only took 255 student hours to complete, although I needed more than double tha amount of full-time employee hours than I originally estimated. Overall, this cost analysis shows a very favorable result to this project, and I am pleased that it fell into the category of underbudget projects.

Table 1. Anticipated vs. Actual Costs

Category	Item	Anticipated Cost	Actual Cost
Labor	280 student hours	$3758	$3422
Labor	6 employee hours	$330	$825
Parts	Components	$800	$488
Parts	Enclosures	$180	$143
Overhead	Lab resources	$150	$150
Total		$5218	**$5028**

7.0 SAFETY AND ETHICAL ASPECTS OF DESIGN

Because of the high-power applications that this device will be associated with, it is important to consider safety and failsafes. Most importantly, the entire circuit is enclosed in a painted steel box which is tied directly to earth groun through the wall outlet power cord. The power lines are fused on both sides of the isolation of the circuit, and a safety relay has been implemented which will short the onboard DC power supply through a 100Ω power resistor at any time when the circuit is not energized. A series of rectifiers ensure that the polarized, high energy-density capacitors will never carry a reverse charge that is so dangerous with those particular capacitors.

In summary, the user should not be in any abnormal danger when operating this variable hardware inductance simulator, as it maintains the same safety standards as any household appliance. The desing includes components that are design to fail safe and be easily replaced in the event of a problem, saving time and money should an accident occur.

8.0 CONCLUSIONS AND RECOMMENDATIONS

Based on extensive testing and simulation, the variable hardware inductance simulator is ready to be integrated into its application area. Results are consistant, and error over the range of possible inductance values is below 5%. Safety concerns have been addressed with redundant failsafes and a secure, grounded enclosure.

The deliverable meets the criteria given at the beginning of the project, and the cost to design it was very close to that which was expected. It is reasonable to project that duplicates will cost much less to contruct due to reduced design and testing costs.

Should the Institute for Technology be interested in simulating smaller inductances, a few simple modifications to this circuit will allow for much higher current limitations.

REFERENCES

[1] Pauker, Vlad. "Gyrator circuit simulating an inductance and use thereof as a filter or oscillator." United States Patent 4812785. 14 Mar. 1989.

[2] Fujii, Tomohiro. "Grounded inductance circuit using a gyrator circuit." United States Patent 5825265. 20 Oct. 1998.

[3] Wikipedia. http://en.wikipedia.org/wiki/Gyrator. Accessed: 02/18/2006. MediaWiki, 2006.

[4] Vanderleest, Steve. http://engr.calvin.edu/courses/engr204/2000/examples/OpAmps. Accessed: 02/18/2006. Calvin College, 2002.

APPENDIX A – CIRCUIT DIAGRAMS

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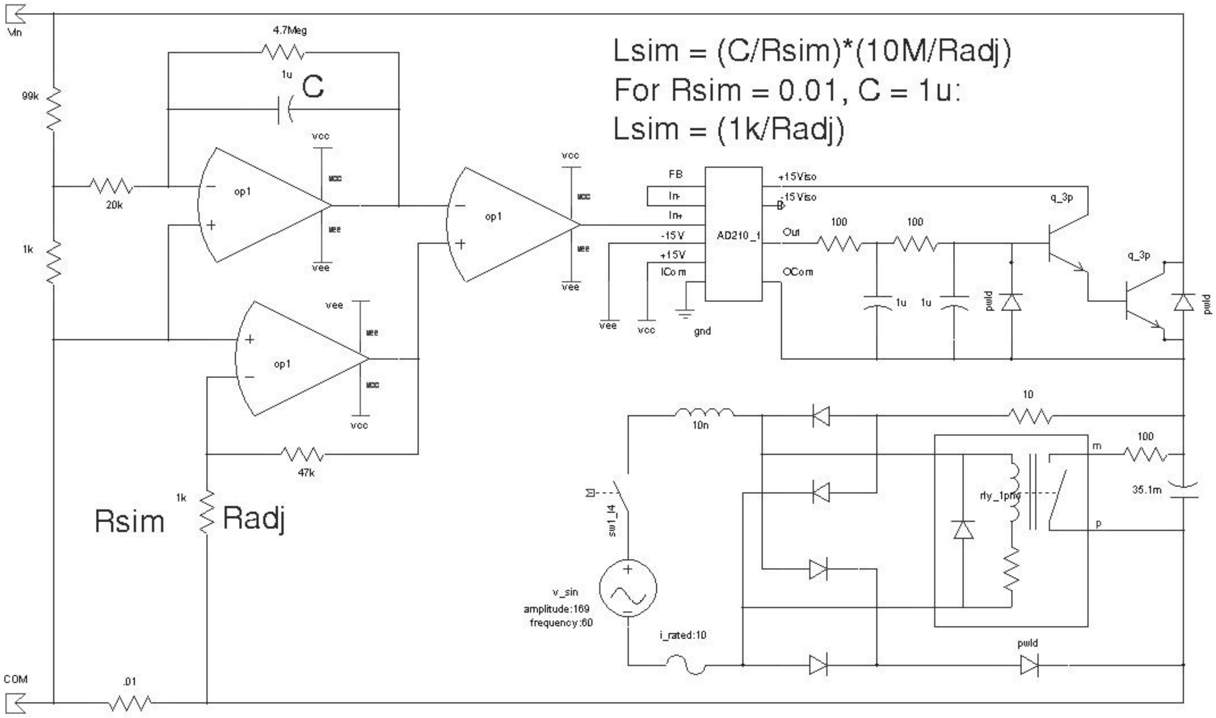
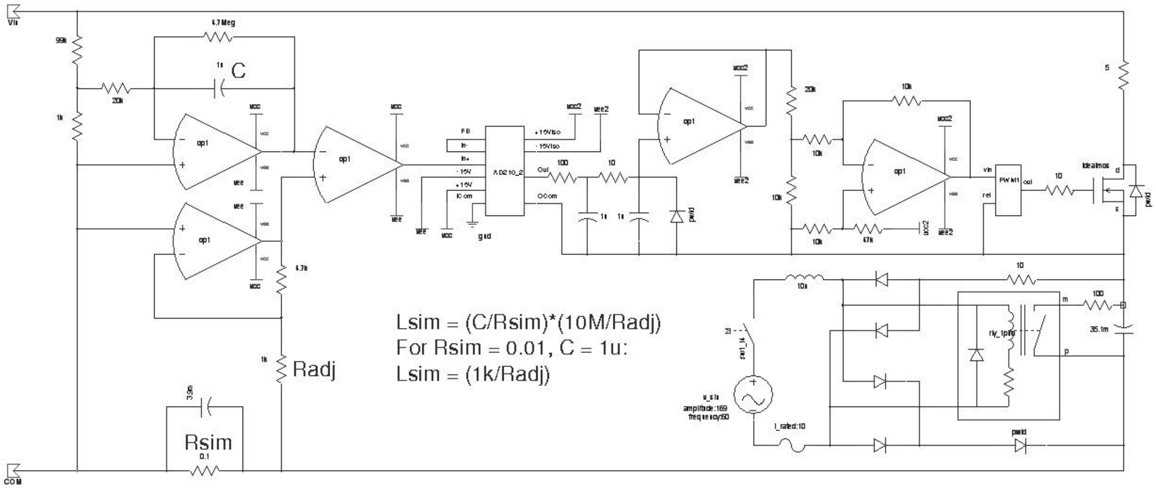


Linear Transistor Circuit Diagram



Switching MOSFET Circuit Diagram